AMENDMENTS TO THE CLAIMS

Claim 1 (previously presented): A method for electrically isolating shallow trenches between components on the surface of a semiconductor wafer comprising:

(a) forming a plurality of first-type trenches and second-type trenches on a semiconductor substrate, each of the first-type trenches having a width greater than a predetermined size that is greater than a width of each of the second-type trenches;

(b) performing a photolithographic process to form at least one photoresist pattern in each of the first-type trenches;

(c) performing an etching process to form at least one dummy and a plurality of third-type trenches in each of the first-type trenches with the photoresist patterns as masks, and to deepen each of the second-type trenches;

(d) stripping the photoresist patterns;

(e) forming a dielectric layer over the surface of the semiconductor wafer, wherein the dielectric material of the dielectric layer fills the first-type trenches, the second-type trenches, and the third-type trenches on the surface of the semiconductor wafer;

(f) condensing the dielectric layer; and

(g) performing a planarization process to polish the surface of the semiconductor wafer for aligning the surface of the dielectric layer inside each of the first-type trenches and the second-type trenches with the surface of each component on the semiconductor wafer.

Claim 2 (previously presented): The shallow trench isolation method of claim 1 wherein the predetermined size is about 2 μm.

Claim 3 (original): The shallow trench isolation method of claim 1 wherein the preferred height of any dummy is around 300 Å to 500 Å.

Claim 4 (original): The shallow trench isolation method of claim 1 wherein the planarization process performed on the dielectric layer surface is a chemical

mechanical polishing process.

Claim 5 (previously presented): The shallow trench isolation method of claim 1 wherein each component on the semiconductor wafer surface comprises a Si substrate, a pad oxide layer above the Si substrate, and a pad nitride layer above the pad oxide layer, and the planarization process performed on the dielectric layer surface makes this surface inside each of the first-type trenches and the second-type trenches align approximately with the pad nitride layer of each component on the semiconductor wafer surface; wherein the shallow trench isolation method further comprises:

performing a second planarization process to strip off the pad oxide layer and pad nitride layer from each component, and make the surface of the dielectric layer inside each of the first-type trenches and the second-type trenches approximately align with the surface of the Si substrate of each component.

Claim 6 (previously presented): The shallow trench isolation method of claim 5 wherein the bottom of each of the first-type trenches and the second-type trenches on the semiconductor wafer is formed by a Si substrate, and each dummy is also made of Si.

Claim 7 (previously presented): The shallow trench isolation method of claim 6 wherein after the second planarization process, the dielectric material formed in each of the first-type trenches remains covered over each Si dummy for electrical isolation.

Claim 8 (original): The shallow trench isolation method of claim 5 wherein the second planarization process is an etch process.

Claim 9 (original): The shallow trench isolation method of claim 5 wherein the pad oxide layer and pad nitride layer are used as a mask or a sacrificial layer during a previous ion implantation or heat diffusion process.

Claim 10 (original): The shallow trench isolation method of claim 1 wherein the dielectric layer is condensed by using an annealing process.

Claim 11 (original): The shallow trench isolation method of claim 10 wherein the dielectric layer is deposited on the surface of the semiconductor wafer by using a chemical vapor deposition process and the dielectric layer comprises $Si(OC_2H_5)_4$ (tetra-ethyl-ortho-silicate, TEOS) in it.

Claim 12 (previously presented): The shallow trench isolation method of claim 1 wherein each dummy is formed at the bottom of each of the first-type trenches.

Claim 13 (Canceled)

Claim 14 (withdrawn): A semiconductor wafer comprising:

a Si substrate;

a plurality of components positioned on the Si substrate, and each pair of neighboring components having a shallow trench between them for isolating the two components;

a dielectric material filled in each shallow trench for electrically isolating the two components on two sides of the shallow trench;

wherein for shallow trenches with widths greater than a predetermined size, at least one dummy is generated at the bottom of each of the shallow trenches to form a plurality of new shallow trenches with widths less than the predetermined size, and the dielectric material filled in each of the shallow trenches covers above each dummy to achieve electrical isolation.

Claim 15 (withdrawn): The shallow trench isolation method of claim 14 wherein the predetermined size for the chosen shallow trenches is 2 μm.

Claim 16 (withdrawn): The shallow trench isolation method of claim 14 wherein the preferred height of any dummy is around 300 Å to 500 Å.

Claim 17 (withdrawn): The semiconductor wafer of claim 14 wherein each dummy is formed of Si, and the method for forming the shallow trenches and the dummies on

the semiconductor wafer comprises:

performing a photolithography and etching method on the surface of the semiconductor wafer down to at least the Si substrate to make the shallow trenches between each component;

applying photoresist to each dummy's position at the bottom of each shallow trench which is wider than the predetermined size;

etching all the shallow trenches on the surface of the semiconductor wafer again to complete all the shallow trenches and the dummies; and

stripping off the photoresists on the semiconductor wafer.

Claim 18 (withdrawn): The semiconductor wafer of claim 14 wherein the method for forming all the shallow trenches and dummies comprises:

using a photomask to define the positions of all the shallow trenches and dummies on the surface of the semiconductor wafer; and

performing a photolithography and etching method to form the shallow trenches and dummies simultaneously.

Claim 19 (withdrawn): The semiconductor wafer of claim 18 wherein when performing the photolithography and etching method, the semiconductor wafer is covered with a photoresist layer, and the photomask contains a plurality of transparent areas with different light penetration capability for defining the positions of all the shallow trenches and the dummies on the semiconductor wafer so that the amount of light emitted through the photomask to the photoresist layer over each shallow trench's position is different from the amount of light emitted to each dummy's position whereby all the shallow trenches and the dummies can be formed at the same time by using the photomask and the photoresist layer.

Claim 20 (withdrawn): A method for forming electrically isolating shallow trenches between components on the surface of a semiconductor wafer comprising:

(a) providing a semiconductor substrate having at least a first-type trench region used to form a first-type trench, and a second-type trench region used to form a second-type trench, the first-type trench having a width

greater than a predetermined value that is greater than a width of the second-type trench;

(b) forming a first photoresist pattern on the semiconductor substrate exposing the first-type trench region and the second-type trench region, and at least a second photoresist pattern on the first-type trench region, the second photoresist pattern having a smaller height than the first photoresist pattern;

(c) etching the first-type trench region and the second-type trench region to form the first-type trench and the second-type trench with the first photoresist pattern as a mask, and to form at least one dummy at a bottom of the first-type trench with the second photoresist pattern as a mask;

(d) stripping the first photoresist pattern and the second photoresist pattern;

(e) forming a dielectric layer over the surface of the semiconductor substrate, wherein the dielectric material of the dielectric layer fills the first-type trench and the second-type trench on the surface of the semiconductor substrate;

(f) condensing the dielectric layer; and

(g) performing a planarization process to polish the surface of the semiconductor wafer for aligning the surface of the dielectric layer inside each of the first-type trench and the second-type trench with the surface of each component on the semiconductor substrate.

Claim 21 (withdrawn): The method of ~~claim 14~~ claim 20 further comprising:

forming a photoresist layer over the semiconductor wafer; and

utilizing an optical mask of different sets of light penetration capability to perform a photolithography process on the photoresist layer for simultaneously forming the first ~~photorsist~~ photoresist pattern and the second photoresist pattern in the photoresist layer.

Claim 22 (withdrawn): The method of ~~claim 14~~ claim 20 further comprising:

forming a photoresist layer over the semiconductor wafer;

exposing the photoresist layer to light through a first optical mask of

different sets of light penetration capability to define the first ~~photorsist~~ photoresist pattern;

exposing the photoresist layer to light through a second optical mask of different sets of light penetration capability to define the second photoresist pattern; and

developing the photoresist layer to form the first ~~photorsist~~ photoresist pattern and the second pattern.

Claim 23 (withdrawn): The method of ~~claim 14~~ claim 20 wherein the predetermined value is about 2 μm.

Claim 24 (withdrawn): The method of ~~claim 14~~ claim 20 wherein a preferred height of any dummy is around 300 Å to 500 Å.